Exhibit Q

Nos. 19-1720, 19-1721, 19-1722, 19-1723, 19-1724

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

GOOGLE LLC, INPHI CORPORATION,

Appellants,

v.

NETLIST, INC.,

Cross-Appellant.

Appeals from the United States Patent and Trademark Office, Patent Trial and Appeal Board in Nos. 95/000,578; 95/000,579; and 95/001,339

RESPONSE BRIEF FOR CROSS-APPELLANT NETLIST, INC.

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DECEMBER 12, 2019

CERTIFICATE OF INTEREST

Counsel for cross-appellant Netlist, Inc. certifies the following:

1. The full name of every party or amicus represented by me is:

Netlist, Inc.

2. The name of the Real Party in interest (Please only include any real party in interest NOT identified in Question 3) represented by me is:

None.

3. All parent corporations and any publicly held companies that own 10% or more of the stock of the party or amicus curiae represented by me are:

None.

4. The names of all law firms and the partners or associates that appeared for the party or amicus now represented by me in the trial court or agency or are expected to appear in this court (and who have not or will not enter an appearance in this case) are:

MORRISON & FOERSTER LLP: David S. Kim.

5. The title and number of any case known to counsel to be pending in this or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal:

Netlist, Inc. v. Google LLC, No. 4:09-cv-05718 (N.D. Cal.)
Netlist, Inc. v. Inphi Corporation, No. 2:09-cv-00690-FMO-RNB (C.D. Cal.)

Dated: December 12, 2019 /s/ Seth W. Lloyd

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STATEMENT OF RELATED CASES

No appeal from these proceedings on U.S. Patent No. 7,619,912 (the '912 patent) involving Google LLC, Inphi Corporation, and Netlist, Inc. has previously been before this Court or any other court. Netlist asserted the '912 patent in *Netlist, Inc. v. Google LLC*, No. 4:09-cv-05718-SBA (N.D. Cal.) and in *Netlist, Inc. v. Inphi Corporation*, No. 2:09-cv-00690-FMO-RNB (C.D. Cal.). Counsel for Netlist know of no other cases pending in this or any other court that will directly affect or be affected by this Court's decision in this appeal.

JURISDICTIONAL STATEMENT

Netlist agrees with Google's and Inphi's jurisdictional statements. Additionally, Netlist moved on December 6, 2019, to voluntarily dismiss its cross-appeals. Dkt. 34. The Court had not acted on that motion before Netlist filed this brief. Thus, although the case-caption identifies Netlist as a cross-appellant, this brief is only a response to Google's and Inphi's appeals.

INTRODUCTION

Netlist did what patent owners are expected to do during a reexamination—it narrowed its claims to define its precise inventive contributions over the prior art. The Board recognized that those contributions are real and patentable, finding the prior art neither discloses nor would have rendered obvious Netlist's memory-module design that provides a cost-effective solution for increasing memory-module capacity. Netlist's patent claims memory modules that allow, for example, a computer system to address modules with double the number of memory devices that the system would otherwise support. The Board found Netlist's comprehensive solution went far beyond the limited approaches taught in the prior art.

Google's and Inphi's appeals fail to justify undoing the nearly decade of work that led to those Board findings. This consolidated *inter partes* reexamination has lasted almost ten years, includes a file history spanning more than 64,000 pages, and has produced three written Board decisions on patentability totaling 166 pages. Yet Google's lead argument is that the Board was required to give it even more process, and on a claim-construction issue to which Google devoted just three sentences at the Board. Inphi leads its appeal with the same claim-construction issue, despite conceding to the Board that the claims carry the meaning the Board gave them.

Even so, the Board's reasoning is clear and correct. Netlist revised its claims to require a memory module with a logic element that acts "in response at least in

part to" four enumerated signals, or "responds at least to" four enumerated signals. The plain and only reasonable reading of that language is that the logic element responds to all four enumerated signals, although it may also respond to other signals. In fact, Netlist unequivocally disclaimed any broader meaning during the reexamination.

Neither appellant musters a convincing substantial-evidence challenge to the Board's findings under that correct construction. Both present one-sided versions of the evidence without grappling with the evidence the Board found went the other way, including often unrebutted declaration statements from Netlist's expert. And both rely on their own expert (or in Inphi's case, its employee), ignoring that the Board found Google's and Inphi's submitted declarations "uncorroborated," and not "persuasive" nor "probative."

The Court should affirm.

STATEMENT OF THE ISSUES

1. Whether the Board correctly gave "logic element . . . wherein the logic element generates" and similar terms their plain meaning.

2. Whether substantial evidence supports the Board's findings that none of the prior art discloses or suggests the disputed element.

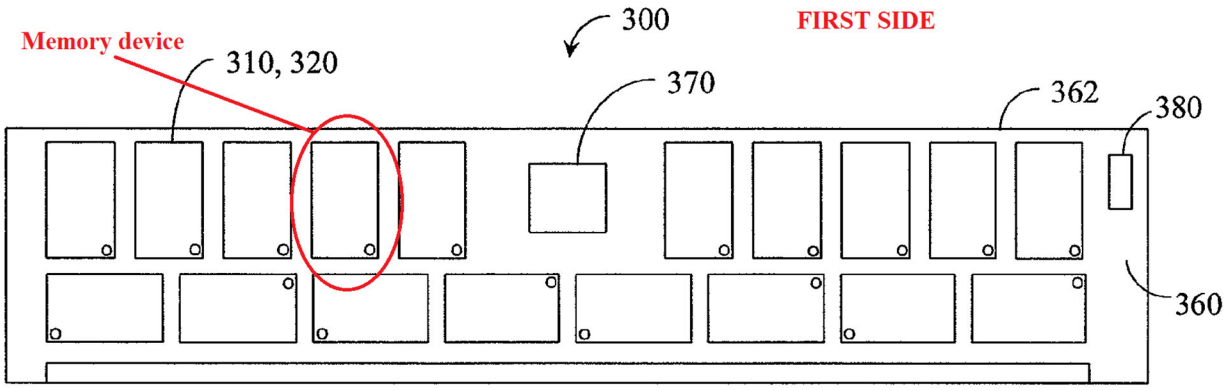
STATEMENT OF THE CASE

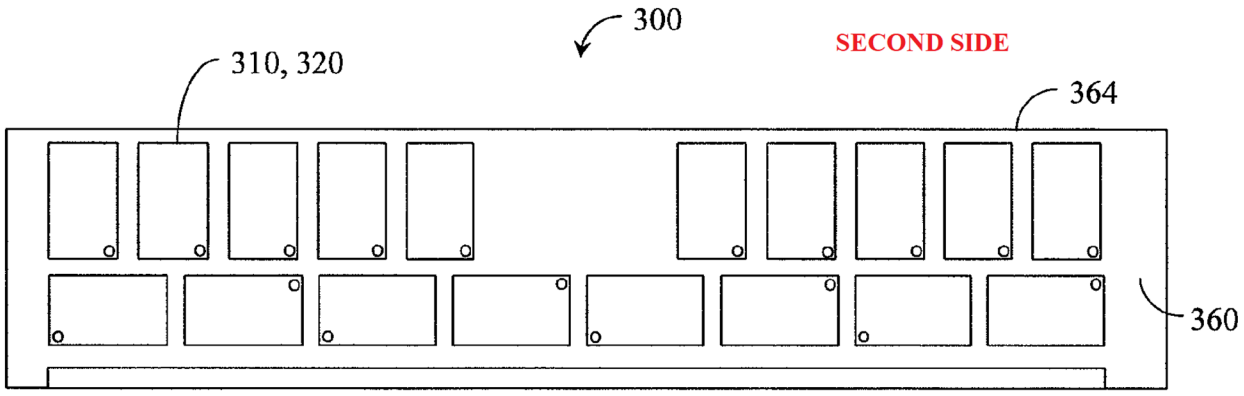
A. Netlist's Groundbreaking Memory Module Design

Netlist is a pioneer in the area of high-performance server memory and has a diverse product line, including the widely praised HyperCloud™ memory module embodying the '912 patent. Appx858-918.

1. Technology background

Memory modules include multiple memory devices (or chips), shown below on first and second sides of exemplary module 300:





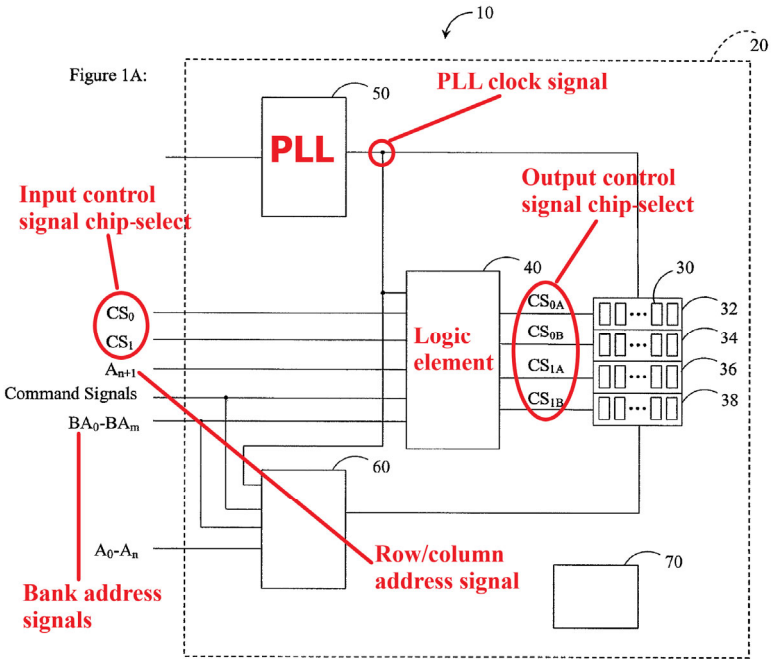
Appx214 (red markings added). These devices can be grouped into "ranks" of memory devices, such as two ranks (one per side) of 18 devices each. Appx214. Each memory device has millions or billions of individual memory cells. Appx218 (col.1:20-col.2:42). The cells are organized into an array (like a grid), which are addressed by specifying the row and column of the desired cell. Appx218 (col.1:20-col.2:42). Sometimes, a single memory device has multiple arrays, called "banks," and each memory cell is addressed by specifying the cell's bank, row, and column. Appx218 (col.1:20-col.2:42). In a typical computer system, the main processor communicates with the memory module via a memory controller—the controller sends chip-select signals to select the rank of memory devices on the module, bank address signals to identify the array within each memory device, and row and address signals to identify the cell within the array. Appx218 (col.1:20-col.2:42).

There are generally two ways to increase the capacity of a memory module, also called module "memory density": increase the number of memory cells per memory device (i.e., increase device memory density), or increase the number of

memory devices per module (such as by increasing the number of ranks). Appx218 (col.1:20-col.2:42). Increasing the number of cells per device often is much more costly than increasing the number of devices per module. Appx219-220 (col.4:59-col.5:5). But the system memory controller's design may limit the number of devices per module—for example, the memory controller may be able to address only a maximum number of devices per module, such as 36 devices organized into two ranks of 18. Appx218 (col.1:20-col.2:42).

2. The '912 patent

The '912 patent teaches the first complete solution to this problem by integrating a sophisticated circuit into the memory module to translate between the system memory controller and the memory devices. Appx223-229 (col.12:12-col.23:25). The patent calls this "memory density multiplication" because "two memory devices having a memory density are used to simulate a single memory device having twice the memory density." Appx223 (col.12:13-15). Annotated Figure 1A from the patent shows a portion of an exemplary memory module:



Appx200 (red markings added). The module (10) includes circuit (20) with a logic element (40), a phase-lock loop (PLL) device (50), and a register (60). Appx200; Appx223 (col.12:25-43). The circuit receives from the system memory controller input control signals corresponding to a virtual memory module with fewer memory devices than the actual module has. Appx200; Appx223 (col.12:25-43). These input control signals include chip-select signals CS_0 and CS_1, address signals A_0-A_{n+1}, and bank address signals BA_0-BA_m. Because the signals are for a virtual memory module with fewer memory devices, the logic element (40) responds to the signals—including to an extra address signal A_{n+1}, bank address signals BA_0-BA_m, and chip-select signals—as well as to a PLL clock signal to generate output control signals for the actual number of memory devices. Appx200; Appx223-229 (col.12:12-col.23:25). In Figure 1A, the logic element generates four new chip-select signals

CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}, as output control signals. Appx200; Appx223-229 (col.12:12-col.23:25).

The specification explains how the logic element uses an "additional address signal bit," which the specification calls a "density transition bit," together with other input control signals to communicate with additional memory devices on the module. Appx223 (col.12:21-25). For example, the virtual memory devices may be organized into two virtual ranks of 18 devices (for a total of 36), each device having four internal banks of 2^{14} rows and 2^{12} columns of memory cells. Appx223-224 (col.12:38-col.14:16). The actual memory devices may be organized into four actual ranks of 18 devices (for a total of 72) with each device having four internal banks of 2^{13} rows and 2^{12} columns of memory cells. Appx223-224 (col.12:38-col.14:16). The input signals for the virtual memory module thus include an extra row address signal (A_{13}). Appx223-224 (col.12:38-col.14:16). Table 1 shows an example of partial logic for a logic element responding to the extra row address signal (A_{n+1}) and other input signals to generate output control signals for the additional ranks of actual memory devices:

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Appx221 (col.7:55-col.8:43); Appx223-224 (col.12:38-col.14:16).

The specification gives other details necessary to resolve the significant complexities required to translate all memory operations between virtual and actual memory devices. Appx223-229 (col.12:12-col.23:25). It explains that, to accommodate "read/write commands," the logic element "latche[s]," meaning stores, the value of the extra row address bit "during the activate command for the selected bank." Appx222 (col.9:18-21). The specification also explains how the logic element avoids "collisions or interference between back-to-back adjacent read commands which cross memory device boundaries." Appx229-233 (col.23:26-col.32:26). Because the system memory controller addresses virtual memory devices, it is unaware of which actual memory device contains which memory cells and thus unaware of the actual "device boundaries." Appx229 (col.23:26-col.24:58). The specification thus teaches ways for the logic element to respond to the input signals by generating output control signals so that "collisions are avoided." Appx229 (col.23:26-col.24:58). The specification also provides exemplary

"Verilog" (a hardware description language) code for a circuit that responds to a row address bit, bank address signals, chip-select signals, and a PLL clock signal by generating output control signals. Appx226-227; Appx924-925 (Netlist's expert explaining same), Appx949-950, Appx919-955.

Google's and Inphi's appeals focus on one claim limitation, which the Board referred to as the "logic element" limitation. Netlist's claims recite slight variations of "logic element" limitations, but Google and Netlist interpret them identically on the disputed issue. For example, claim 1 recites:

> a logic element . . . wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal.

Appx16758-16759. Other claims like claim 52 omit "in part," among other variations:

> a logic element . . . wherein the logic element responds to at least (i) a row address bit of the at least one row/column address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a first number of chip-select signals of the set of output control signals.

Appx16782-16783; *see* Appx16787-16789 (claim 67); Appx16790-16792 (claim 77); Appx16793-16794 (claim 82); Appx16795-16797 (claim 87).

B. The Board Confirmed Netlist's Claims' Patentability

Inphi, SMART Modular Technologies and Google filed separate requests for *inter partes* reexamination, which the Board granted and consolidated into a single proceeding. After nearly ten years of reexamination, the Board affirmed the patentability of dozens of Netlist claims in a 43-page decision. Appx111-153. By the Board's own reckoning, it reviewed 15 declarations, 8 prior-art references, and 7 grounds of rejection from 3 different third-party requesters. Appx116-119, Appx148. And that was for only one of the Board's patentability decisions; the Board had already issued a hundred-plus page decision addressing many other grounds and references, and later issued a decision on rehearing. Appx4-108; Appx154-165.

1. The Board construed "in response at least in part to" enumerated signals and similar phrases to require responding to all enumerated signals

As relevant here, the Board's decisions interpreted limitations like a "logic element . . . wherein the logic element is responsive at least in part to" enumerated signals to mean the logic element must respond at a minimum to all enumerated signals. For example, the Board's first decision addressed claim 52, which then recited a "logic element . . . wherein the logic element responds to at least a row address bit of the at least one row/column address signal, the bank address signals, and the at least one chip-select signal by generating a first number of chip-select

signals." Appx6636-6637; Appx746-826; Appx2794-2858; Appx6614-6676. The Board explained that claim 52 "recites a logic element generating a CAS or chip-select signal in response in part to an input bank address signal," that is, the claimed logic element must respond to bank address signals, among other things. Appx73-74. The Board held prior art that failed to disclose a logic element generating a recited output signal "*in response* at least in part to a bank address signal" failed to anticipate. Appx73-74 (emphasis by Board).

Similarly for claim 1, which at the time recited a logic element that generates "chip-select signals of the output control signals in response at least in part to a bank address signal," the Board held that the Examiner's "construction of this phrase is reasonable"—"'[i]f the bank signal is not used in any way to generate the output signals, the generation of output signals cannot be in response to the bank signal.'" Appx77-78 (quoting Examiner). The Board explained that such language requires "that the signal was used in some fashion or 'in part' to generate the output signals." Appx90-91.

Following the Board's first decision, and despite disagreeing with the Board's and Examiner's rejections (Appx16813), Netlist amended independent claims 1, 15, 28, 39, 52, 67, 77, 82, and 87 to recite variations of "a logic element . . . wherein the logic element generates" output signals, like "chip-select signals," "in response at least in part to" four enumerated signals: "(i) the at least one row address signal,

(ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal." Appx16758-16797, Appx16757-16815. Applying the Board's adopted construction of "in response at least in part to" and similar language, Netlist distinguished its amended claims over prior art that failed to disclose or suggest a logic element responding to all four enumerated signals. Appx16808-16811, Appx16803-16814. Inphi conceded that the amended logic element "requires" responding to all four enumerated signals. Appx16901, Appx16893-16969. Google's response to Netlist's request to reopen prosecution asserted in three sentences that "the broadest reasonable interpretation of that phrase is that the CAS and chip select signals are produced in response to 'at least one of' the four enumerated signals" and urged the Examiner to adopt that interpretation. Appx16873, Appx16863-16884. Although the Examiner never adopted Google's construction, Google failed to renew its interpretive challenge after the Examiner's decision. Appx115; Appx18242-18264.

The Board's second decision maintained its earlier interpretation: "as now claimed, claim 1 recites the logic element 'generates chip-select signals' in response to signals (i)-(iv)." Appx123-124; Appx128-129 (similar). Applying that interpretation, the Board repeatedly distinguished prior-art references that "collectively do not teach or suggest sufficiently to one skilled in the art the 'logic element' limitation generating CAS signals in response to both a row address signal

(i.e., signal (i)) and bank address signals (i.e., signal (ii)) as well as signals (iii) and (iv)." Appx128-129; Appx130-131 (similar); Appx134 (similar); Appx136-137 (similar); Appx143-144 (similar).

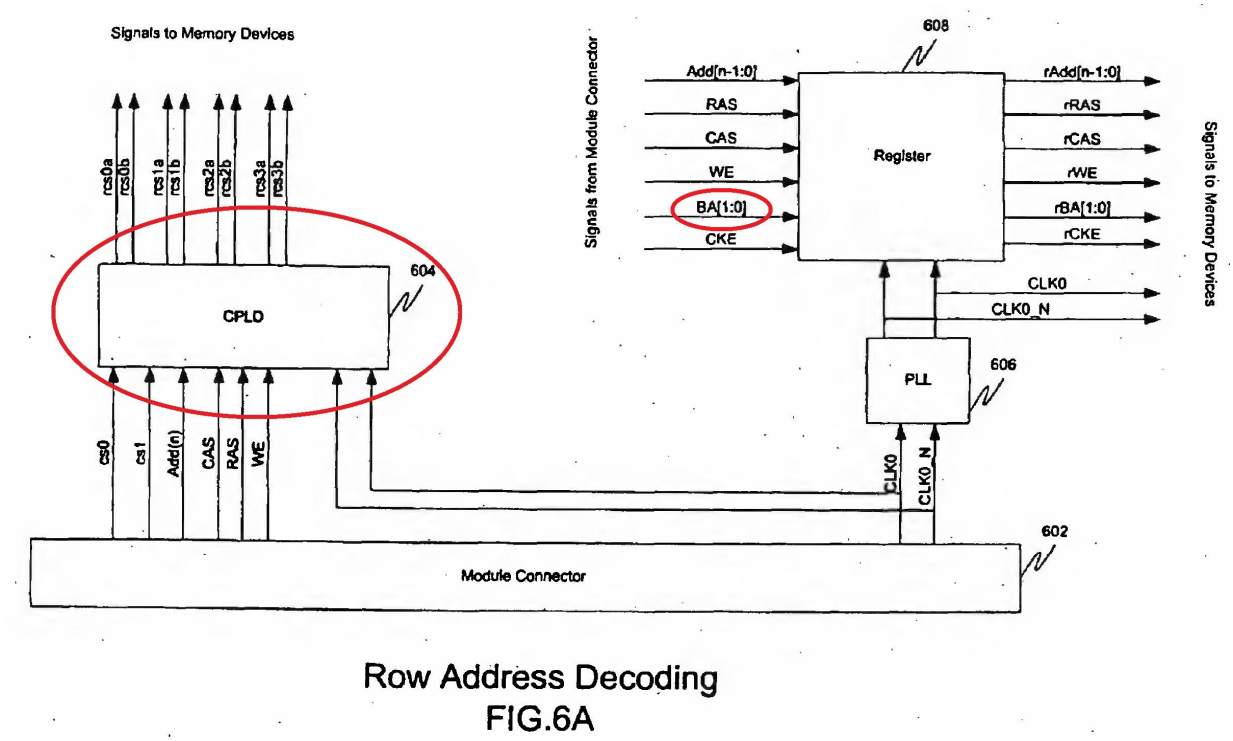
When Google argued on rehearing that "[t]he specification does not support using all four signals together to generate a CAS or chip-select signal" (Appx18743, Appx18737-18748), the Board held Google forfeited the issue. Appx163-164. The Board repeated that it "construed the 'logic element' limitation in the conjunctive," meaning the logic element responds to all four enumerated signals. Appx163 (citing Appx123-124, Appx128-129).

2. The Board found that no prior art discloses or suggests the claimed "logic element" limitation

Focusing on the disputes over the "logic element" limitation, the Board found Netlist's amended claims patentable over, as relevant here, Amidi, Dell 2, JEDEC 21C, Micron, Olarig, and JEDEC 79C. Appx111-153.

a. Amidi, Dell 2, and related references

On Amidi and Dell 2, the Board found Amidi discloses a complex programmable logic device (CPLD) which the requesters alleged was equivalent to the claimed logic element and which "generates chip-select signals in response to both signals (i) [row address signal] and (iii) [input chip-select signals] in claim 1":



Row Address Decoding
FIG.6A

Appx123-124; Appx438 (showing row address signal Add(n), input chip-select signals cs0-cs1, output chip-select signals rcs0a-rcs3b, and bank address signals BA[1:0]; markup added), Appx430-447. The Board reaffirmed its finding from the first decision that "Amidi 'fails to describe or show . . . a bank address signal entering CPLD'" 604, and thus fails to disclose generating chip-select signals in response to bank address signals. Appx124 (quoting Appx23, Appx39).

The Board found that Dell 2 neither supplied the missing pieces nor would have suggested them in combination with Amidi. The Board found that Dell 2, shown below, "teaches a logic circuit (e.g., a switch circuit) that performs a remapping function (e.g., 50) of at least one address signal (e.g., A12) to an

additional bank address signal (e.g., BA1) at CAS [column access strobe] time to ensure the correct *bank* is addressed":

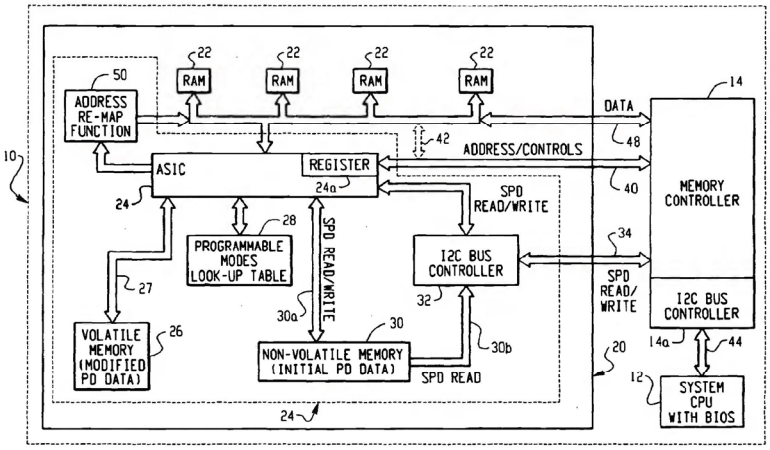


Fig. 1

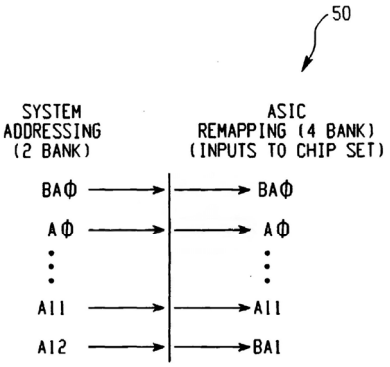


Fig. 1A

Appx126 (emphasis by Board); Appx2301-2302, Appx2299-2309. From this, the Board found "one skilled in the art would have recognized using a logic element, like Amidi's CPLD, to generate a control signal in response to a bank address signal for navigating to the correct *bank* during bank expansion (e.g., generate *bank-select* signals in response to bank address signals)." Appx126 (emphasis by Board).

Yet the Board found that nothing in Amidi or Dell 2, nor any other evidence submitted by the requesters, "sufficiently address[es] why one skilled in the art would have recognized a CPLD, like Amidi's, (e.g., a logic element) generates *chip-select* signals in response to received bank address signals and the other recited signals (i.e., signals (i), (iii), and (iv) recited in claim 1"). Appx126-127 (emphasis by Board). "The above-discussed teachings are inadequate to suggest generating *chip-select* signals (e.g., rank select signals) in response to both a row address signal

and bank address signals as recited in claim 1." Appx127 (emphasis by Board). The Board credited the conclusion of Netlist's expert, Dr. Sechen, that "'[t]here is no disclosure or suggestion [in Dell 2] of using [a] bank address to generate a control signal, such as a chip-select signal or a CAS signal.'" Appx127 (quoting Appx59431, Appx59423-59462). In contrast, the Board twice declined to "find Dr. Wang's [Inphi's employee's] testimony persuasive in teaching or suggesting generating a CAS signal in response to a chip-select signal." Appx128-129; Appx83 (Board did "not find this evidence probative" because "no evidence to support" it).

On JEDEC 21C, the Board found Inphi relied on JEDEC 21C only as suggesting "transmitting PLL clock signals to a CPLD, which "does not cure the above-noted deficiencies in Amidi and Dell 2." Appx130.

b. Micron, Amidi, and related references

On Micron and Amidi alone or combined with Olarig or Dell 2 and JEDEC 79C, the Board found similar deficiencies. Appx133-149. Amidi was deficient for the reasons the Board already found—"the evidence of record does not teach or suggest generating the specifically recited chip-select signals using more than one bank address signal and, more particularly, both bank address signal*s* (i.e., signals (ii)) and a row address signal (i.e., signal (i)) as well as signals (iii) and (iv) claimed in claim 1." Appx136-137.

The Board also rejected Google's inherency theory of obviousness which depended on two unsupported assertions: (1) to generate chip-select signals in response to a row address signal, as in Amidi, "'the rank-multiplying module must store information from row address time'" for later use; and (2) "'[i]nput bank address signals are necessary to determine which stored row address bit should be used to generate chip-select signals'" at that later time. Appx137 (quoting Appx59606, Appx59500-59612); Appx137-144. The Board found Amidi contradicts that theory because, despite showing other elements receiving bank address signals as input, Amidi never "show[s] or suggests bank address signals entering CPLD 604." Appx137-138.

The Board also found Google's expert's "testimony conflicts with Requester 3's [Google's] position" because the expert stated that "'bank address [*sic*] are not always necessary in order to determine the output control signals.'" Appx138 (quoting Appx2287, Appx2275-2298). Although the expert later offered statements purporting to support Google's position, the Board found that the expert "does not discuss how the stored address bits are located" later "such as by using bank address signals as Requester 3 asserts." Appx138-139. Likewise, the Board found the expert's later statements "clash[] with his earlier testimony" in which he explained that bank address signals are unnecessary. Appx140-141 (citing Appx2287). Weighing the totality of this evidence, the Board found that Google's

obviousness theories are "not corroborated sufficiently by Dr. Kozyrakis," Google's expert. Appx141-142; Appx143 (Google's and its expert's later statements "lack[] sufficient corroborating evidence").

In contrast, the Board found that Netlist's expert "Dr. Sechen provides countering evidence and arrives at the opposite conclusion." Appx142-143. The Board found that Amidi's and Micron's express disclosures corroborate Dr. Sechen's conclusions. Appx142-143. The Board concluded, "Weighing all the evidence in the record, we determine one skilled in the art would not have recognized using a known logic element, such as Amidi's, to generate chip-select signals in response to" all four enumerated signals "as recited in claim 1." Appx143-144.

The Board found nothing in Olarig requiring a different conclusion when combined with Micron and Amidi. Appx144-147. As shown below, Olarig discloses remapping a bank address signal (BA0 or BA1) as a row or column address signal (A12 or A10) to translate between memory devices with multiple memory banks and memory devices without banks:

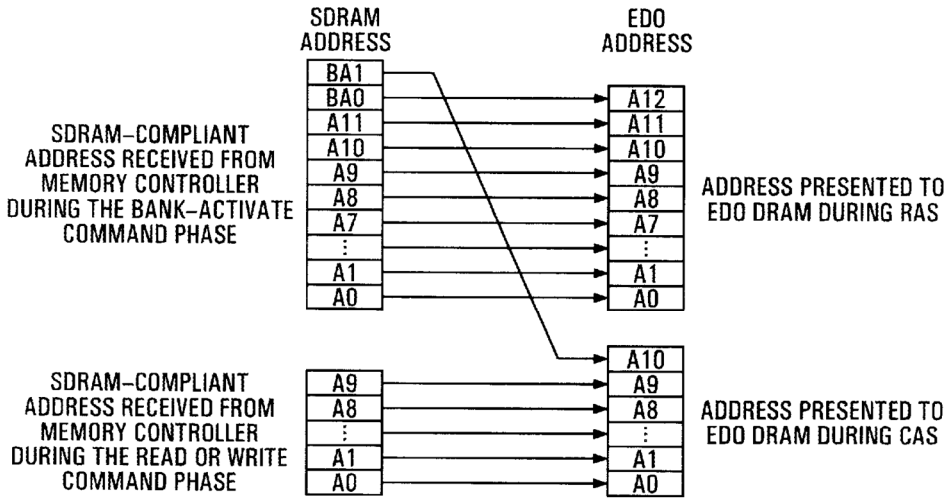


FIG. 6

Appx7402, Appx7396-7429; Appx144-146. The Board found that Olarig, alone or combined with Micron and Amidi, "falls short of suggesting generating a control signal, such as a chip-select signal, in response to both at least one row address signal (e.g., recited signal (i)) and bank address *signals*." Appx145-146 (emphasis by Board). The Board relied on Dr. Sechen's well-supported opinion reaching the same conclusion, to which Google "provides no rebuttal." Appx147.

Finally, the Board found nothing in JEDEC 79C to overcome the deficiencies already found in the other art: "Regarding JEDEC 79C, Requester 3 [Google] does not explain how this reference is being relied upon in its Appeal Brief," and "d[id] not address JEDEC 79C" in its earlier comments. Appx149. The Board "thus determine[d] Requester 3 has not sufficiently demonstrated how JEDEC 79C teaches

or suggests the claimed features missing from Micron, Amidi, and Dell 2." Appx149.

SUMMARY OF ARGUMENT

A. The Board correctly gave the "logic element" limitation its plain meaning. Google's procedural challenge fails because the Board was express that it "construed the 'logic element limitation' in the conjunctive." Appx163. It repeatedly cited the claim text as supporting that understanding. Especially given Google's bare three-sentence argument on the issue before the agency, the Board's explanation was at least commensurate with Google's own treatment.

On the merits, the phrases "in response at least in part to" and "responds to at least" enumerated signals require a logic element that responds, at a minimum, to all enumerated signals. Other claim language confirms that by requiring the logic element to receive all enumerated signals. The specification repeatedly describes logic elements that respond to all enumerated signals. And Netlist clearly and unmistakably disavowed any broader meaning. Google and Inphi argue against the claims' plain meaning by misreading the specification, such as by narrowly reading exemplary embodiments to argue they contradict the Board's construction.

B. Substantial evidence supports the Board's findings that none of the prior art discloses or suggests a memory module with the logic element limitation as properly construed. As Inphi concedes, neither Amidi nor Dell 2 disclose a logic

element responding to a row address signal, bank address signals, chip-select signal(s), and a PLL clock signal. Nor does any evidence show the art would have suggested such a logic element. The Board credited Netlist's expert on that point and found the declaration from Inphi's employee not "persuasive" nor "probative." Inphi ignores that finding, which alone dooms Inphi's challenge.

For similar reasons, substantial evidence supports the Board's findings about combinations involving Micron and Amidi. Google rehashes its inherency argument, that skilled artisans would have recognized that input bank address signals are needed to generate output chip-select signals. A mountain of evidence supports the Board's finding rejecting that theory as uncorroborated, including statements from Google's own expert that "bank address signals are not needed to generate any output control signals." Appx2287. And like Inphi, Google ignores and thus fails to show any error in the Board's crediting of contrary statements from Netlist's expert.

C. Even were the Court to find prejudicial error, remand would be required. The Board decided only the parties' disputes over the logic element limitation, which was enough to confirm the patentability of Netlist's claims. Because the parties also disputed other claim limitations, including the amended register limitation, remand would be required for the Board to resolve those disputes in the first instance.

STANDARD OF REVIEW

The Court reviews Board conclusions of law de novo and findings of fact for substantial evidence. *In re Gartside*, 203 F.3d 1305, 1316 (Fed. Cir. 2000). Claim construction is a question of law that may involve underlying fact finding. *Teva Pharm. USA v. Sandoz*, 135 S. Ct. 831, 838 (2015). The scope and content of the prior art and the differences between the art and the claimed invention are factual issues. *Graham v. John Deere*, 383 U.S. 1, 17 (1966).

ARGUMENT

A. The Board Correctly Gave The "Logic Element" Limitation Its Plain Meaning

Google and Inphi fail to show any procedural or substantive error in the Board's construction of what it called the "logic element" limitation. During the reexamination, Netlist amended its claims to require a logic element that generates specific output signals "in response at least in part to," or "respond[s] to at least," "(i) the at least one row address signal, (ii) the bank address signals," "(iii) the at least one chip-select signal," and "(iv) the PLL clock signal." Appx16758-16797 (the "logic element" limitation). The Board correctly gave that text its plain meaning, which requires a logic element that generates specific output signals in response to all four enumerated signals, although it may also respond to other signals.

1. The Board adequately explained its decision with one hundred and sixty-plus pages of reasoning

Unsatisfied with nearly a decade of extra examination of Netlist's patent and three Board decisions spanning more than one hundred and sixty pages, Google leads its appeal by arguing that the Board's claim construction is defective because the Board failed to follow the Administrative Procedure Act. Google Br. 34-41. Google fails to cite a single provision of that Act that the Board allegedly violated, and there is none. The Board addressed the many issues before it, set forth its conclusions of law, and explained its findings of fact. The Act requires no more.

a. The Administrative Procedure Act requires only adequate explanation under the circumstances, which the Board gave

Under the Administrative Procedure Act, the Court reviews Board decisions to ensure they are not "arbitrary, capricious, an abuse of discretion," or "unsupported by substantial evidence," all while giving "due account" to "the rule of prejudicial error." 5 U.S.C. § 706. To enable that review, the Board "must set forth its findings and the grounds thereof, as supported by the agency record, and explain its application of the law to the found facts." *In re Applied Materials*, 692 F.3d 1289, 1294 (Fed. Cir. 2012) (citation omitted). But nothing "require[s] that agencies explicitly spell out their rationale or reasoning in perfect detail or clarity." *Swagway v. Int'l Trade Comm'n*, 934 F.3d 1332, 1342-43 (Fed. Cir. 2019). Rather, courts must "uphold a decision of less than ideal clarity if the agency's path may reasonably

be discerned." *Bowman Transp. v. Arkansas-Best Freight Sys.*, 419 U.S. 281, 286 (1974). This Court thus affirms even "cryptic" but reasonably discernable Board decisions. *In re Huston*, 308 F.3d 1267, 1280-81 (Fed. Cir. 2002).

The Board's reasoning here is far from cryptic. The Board was express that it "construed the 'logic element limitation' in the conjunctive." Appx163 (citing Appx123-124, Appx128-129). In adopting that construction, the Board repeatedly cited the amended claims' plain language: "as now claimed, claim 1 recites the logic element 'generates chip-select signals' in response to signals (i)-(iv)." Appx123-124 (quoting amended claim 1); Appx128-129 (similar). It explained that the prior-art references "collectively do not teach or suggest sufficiently to one skilled in the art the 'logic element' limitation generating CAS signals in response to both a row address signal (i.e., signal (i)) and bank address signals (i.e., signal (ii)) as well as signals (iii) and (iv)." Appx128-129. The Board repeated that reasoning throughout its decision. Appx130-131; Appx134; Appx136-137; Appx143-144. The Board thus set forth its understanding that the amended claims' text requires a "logic element" that generates a named output signal "in response to" all four signals (i)-(iv). Appx123-124; Appx128-129; Appx163.

The Board's explanation also is adequate because it is "commensurate with" Google's "cursory argument" on the issue. *Novartis AG v. Torrent Pharms. Ltd.*, 853 F.3d 1316, 1327-28 (Fed. Cir. 2017). In *Novartis*, the Court refused "to find

fault in the Board's arguably limited treatment" of motivation to combine where the appellant failed to "direct the Board" to the arguments and record evidence that it pressed on appeal. *Id.*

The Board's decision here was at least commensurate with the third-party requesters' cursory treatment of claim construction at the Board. Inphi conceded the issue. Appx16901-16904, Appx16909; *infra* pp. 29-31. And before the Board issued its second appeal decision, the entirety of Google's argument on the issue was three sentences:

> The Logic Amendment requires the generation of CAS or chip select signals in response "at least in part to" four enumerated signals. The broadest reasonable interpretation of that phrase is that the CAS and chip select signals are produced in response to "at least one of" the four enumerated signals. Accordingly, the claim is disjunctive and therefore rendered obvious if the CAS or chip select signals are generated in response to any of the four enumerated signals.

Appx16873 (citation to Appx220 (col.6:61-62) and emphasis omitted). Google included those three sentences only in its brief "request[ing] that the Examiner reject" the amended claims on remand from the Board. Appx16866. Although the Examiner never adopted Google's construction, Google declined to file a brief renewing its claim construction request before the reexamination returned to the Board. Appx115; Appx18242-18264. After the Board issued its second decision Google requested rehearing by arguing for the first time that "[t]he specification does

not support using all four signals to generate a CAS or chip-select signal." Appx18743. The Board concluded that was a backdoor attempt to raise "a new argument" about a lack of written description, which was "improper" under the Board's rules. Appx163-164. Thus the totality of Google's argument on claim construction was a conclusory assertion that the claims should be rewritten to recite "at least one of" the four enumerated signals and a forfeited written description challenge. Under these circumstances and as in *Novartis*, the Board's repeated explanations throughout all three decisions were more than adequate. 853 F.3d at 1327-28; *LG Elecs. v. Conversant Wireless*, 759 F. App'x 917, 924-25 (Fed. Cir. 2019) (rejecting similar procedural argument for similar reasons). That is especially true under the circumstances here, where the disputed issue is a claim construction based solely on intrinsic evidence which this Court will review without deference. *HTC v. Cellular Commc'ns Equip.*, 877 F.3d 1361, 1367 (Fed. Cir. 2017).

b. Google relies on factually distinct cases and invents ambiguity where there is none

None of Google's cited cases involves similar facts or requires a different result. *Contra* Google Br. 34-41. This is not a case where the Board "focused on a red herring" rather than a party's "primary argument," as in *Power Integrations v. Lee*. 797 F.3d 1318, 1324-25 (Fed. Cir. 2015). Instead of making claim construction a "primary" issue, Inphi failed to raise it at all, and Google did so only in cursory

fashion. Appx115; Appx16873. Nor is this a case where the Court "simply do[es] not know what claim construction the trial judge gave the terms in the claims," as in *Graco v. Binks* 60 F.3d 785, 791 (Fed. Cir. 1995). As Inphi admits, and Google never disputes, the Board "made clear that it construed the claim as requiring all four signals (i)-(iv)." Inphi Br. 29; Google Br. 34-41. The Board expressly stated that conclusion. Appx163.

This case also is unlike *VirnetX v. Cisco Sys.*, *In re Van Os*, or *Rovalma S.A. v. Bohler-Edelstahl GmbH*, cases in which the Board "failed to address" predicate factual issues underlying its conclusions. *VirnetX*, 776 F. App'x 698, 702-03 (Fed. Cir. 2019); *Van Os*, 844 F.3d 1359, 1362 (Fed. Cir. 2017); *Rovalma*, 856 F.3d 1019, 1024-26 (Fed. Cir. 2017). The claim construction issue here required no predicate factual findings, and the Board addressed the relevant issue when it "construed the 'logic element' limitation in the conjunctive." Appx163. The facts here also are nothing like those in *Gechter v. Davidson*, where the Board's decision included only three sentences explaining the ground of unpatentability and failed to address all issues necessary to find anticipation. 116 F.3d 1454, 1459-60 (Fed. Cir. 1997). The Board explained its reasoning for holding the claims patentable here with much more than three sentences, and the dispute over "logic element" was alone sufficient to resolve patentability. Appx1-166.

Nor is Google correct that the Board's decision is ambiguous. Google Br. 37-41. Google bases its entire argument on a red herring about whether "the Board required signals (i) and (ii) to *simultaneously* serve as density transition bits." Google Br. 38. Google's three-sentence assertion about claim construction made no mention of "density transition bits," neither Board decision after Netlist amended the claims refers to such bits, and the disputed "logic element" limitation never uses that term even though other claims do. Appx109-166; Appx16770 (claim 22). The Board's decision thus contains no ambiguity about "density transition bits" because that term was not even part of the conversation.

Google is wrong (at Br. 38) that Netlist's arguments at Appx16810 left any doubt about the meaning of "logic element." Netlist was unambiguous that the logic element must "use both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal[s]." Appx16810. The Board was unambiguous in agreeing with that reasoning: it found the prior art fails "to suggest generating *chip-select* signals (e.g., rank select signals) in response to both a row address signal and bank address signals as recited in claim 1." Appx127 (emphasis by Board); Appx133-144.

Google misstates the issue in discussing the reexamination history surrounding what Google calls the "first case" and "second case." Google Br. 37-38. The comments to which Google points are about a different claim amendment

requiring the logic element to receive "at least one row address signal" "separate from" the "row/column address signals received by the register." Appx16804, Appx16810. Netlist explained that this amendment requires "a logic element separately receiving a row address signal (i.e., similar to the first case)," as Google used that term. Appx16810. Because Google's "second case" involved no extra row address signal, Netlist explained that the claim amendment "exclude[s] the second case involving one more bank address signal." Appx16810. Google's "second case" never "receives at least one row address signal separate from the address signals received by the register." Appx16810. Regardless of whether the Board agreed with Netlist, nothing about these comments makes the Board's explanation of a logic element responding to all four enumerated signals ambiguous because the comments are about a different claim requirement.

2. The broadest reasonable interpretation requires a logic element that responds to all four enumerated signals

On the merits, the Board correctly construed the claimed logic element as generating the recited output in response to all four enumerated signals.

a. Inphi conceded to the construction the Board adopted and cannot change tunes now

When a party agrees to or at least never disputes a construction before the Board, this Court refuses on appeal to consider any claim construction challenge from that party. *Elbit Sys. v. Thales Visionix*, 881 F.3d 1354, 1357 n.3 (Fed.

Cir. 2018); *Palo Alto Networks v. Finjan*, 752 F. App'x 1017, 1022-23 (Fed. Cir. 2018).

This law ends Inphi's attempt to challenge the Board's construction of "logic element." At the Board, Inphi conceded the construction the Board adopted, that Netlist's claim amendments "require[]" the logic element respond to all four enumerated signals. Appx16901-16904, Appx16909. Inphi argued that the amendment created a "requirement that the logic element generates gated CAS or chip-select signals in response to bank address signals and the PLL clock signal," and also "requires that the logic element generates the gated CAS or chip-select signals in response to 'the at least one row address signal' and in response to 'the at least one chip-select signal.'" Appx16901. It similarly argued that "the third wherein clause," meaning the disputed amendment to the logic element, "specif[ies] that the logic element generates gated CAS or chip-select signals . . . in response to input chip-select signals, at least one row address signals [*sic*] and bank address signals." Appx16909. Nowhere did Inphi dispute that the logic element must respond to all four signals or argue, as it now does, that the claims cover a logic element that responds to any one of the four enumerated signals. Appx16891-16969.

It thus is far too late for Inphi to argue for a different claim scope. *Elbit*, 881 F.3d at 1357 n.3; *Palo Alto*, 752 F. App'x at 1022-23. That is true even if Google's three-sentence argument is enough for Google to have preserved the issue on appeal.

Although this Court consolidated these appeals for administrative convenience, Inphi's appeal is still a separate appeal involving separate Board grounds of unpatentability. *Compare* Inphi Br. 49 (citing "Ground 5 and new grounds of rejection"), *with* Google Br. 57 (citing Grounds 13, 19, and 21). As to that appeal on those grounds, the law prohibits Inphi from conceding to one construction before the Board while alleging error on appeal by arguing for a different construction.

b. The claim text, specification, and prosecution history support only one reasonable interpretation

As to the proper construction, the Board correctly followed the rule that even under the broadest-reasonable-interpretation standard a claim term's plain meaning governs absent redefinition or disavowal. *Straight Path IP Grp. v. Sipnet EU S.R.O.*, 806 F.3d 1356, 1360-61 (Fed. Cir. 2015). Amended claim 1 of Netlist's '912 patent requires, among other things:

> a logic element . . . wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal.

Appx16758-16759; Appx115-116. Other challenged claims recite a similar limitation without the "in part" language:

> a logic element . . . wherein the logic element responds to at least (i) a row address bit of the at least one row/column address signal, (ii) the bank address

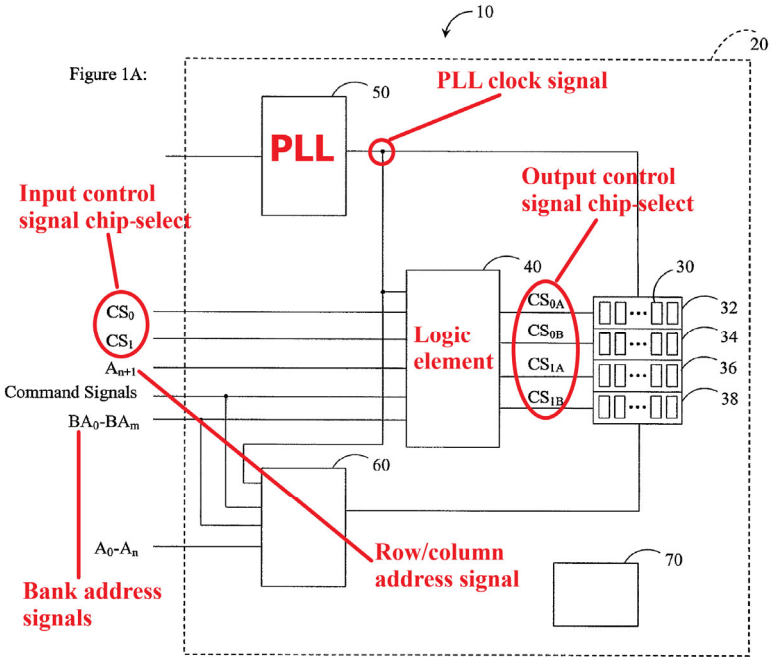
> signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a first number of chip-select signals of the set of output control signals.

Appx16782-16783 (claim 52); *see* Appx16787-16789 (claim 67); Appx16790-16792 (claim 77); Appx16793-16794 (claim 82); Appx16795-16797 (claim 87).

The meaning of this text is plain. The claims require a logic element that generates an output signal "in response at least in part to" four enumerated signals, or "responds to at least" four enumerated signals "by generating" an output signal. Appx16758-16783. That means the logic element generates the output signal in response to all four enumerated signals. The logic element may also respond to other signals, but it must "at least" respond to the four enumerated signals.

Further confirming that "conjunctive" meaning, each relevant claim separately requires the logic element to receive all four enumerated signals. The logic element must "receiv[e] a set of input control signals . . . comprising at least one row/column address signal, bank address signals, and at least one chip-select signal," as well as a "PLL clock signal." Appx16758-16759; Appx16782-16797 (similar for other claims). The claims thus require the logic element to receive all four enumerated signals so it can respond to all four of them. And the claims are express that the logic element may receive other signals, just as they are express that it may respond to other signals. Appx16758-16797.

The specification reinforces this meaning. For example, Figure 1A illustrates a logic element receiving all four enumerated signals and outputting chip-select signals in response:



Appx200 (markup added); Appx220-221 (col.5:22-45, col.7:36-53). Other figures in the patent are similar. Appx201, Appx203-204. The specification explains that "the logic element 40 receives a set of input control signals, which include address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals)"; the logic element also receives "clock signals" that "the phase-lock loop device 50 transmits." Appx220 (col.5:28-31, col.6:55-61). "In response to the set of input control signals, the logic element 40 generates a set of output control signals" such as new chip-select signals. Appx220-221 (col.6:61-col.7:19); Appx221 (col.7:36-53) (similar); *see* Appx228-

229 (col.22:50-col.23:25) (discussing generating gated column access strobe signals).

The specification also explains how the logic element responds to input signals to generate an output signal. For example, in some embodiments the computer system sends control signals with one more row address bit than the actual memory devices support. Appx200-201 (A_{n+1} in Figures 1A and 1B), Appx221 (col.7:36-53), Appx223-224 (col.12:12-14:4). The logic element translates this extra address bit to address the actual memory devices. Appx221-222 (col.7:36-col.9:21). To do so, the logic element responds to more than just the extra row address bit: it "latche[s]," meaning stores, the value of that bit "during the activate command for the selected bank." Appx222 (col.9:18-21). That requires at least responding to the PLL clock signal ("*during* the activate command") and the bank address signals ("*selected* bank"). Appx222 (col.9:18-21) (emphases added). The specification provides exemplary "Verilog code" for a logic element responding to all these signals. Appx226-227 (Example 2). Netlist's expert Dr. Sechen similarly explained how the specification teaches skilled artisans to use all four signals to generate the recited output signals. Appx924-925, Appx949-950.

The prosecution history, like the other intrinsic evidence, leaves no reasonable doubt that the claims require a logic element that generates the output signal in response to all four enumerated signals. Statements made during

"reissue/reexamination proceeding[s]" are "relevant prosecution history when interpreting claims." *E.I. du Pont de Nemours v. Phillips Petro.*, 849 F.2d 1430, 1439 (Fed. Cir. 1988). Thus "[a] patentee's statements during reexamination can be considered during claim construction." *Krippelz v. Ford Motor*, 667 F.3d 1261, 1266 (Fed. Cir. 2012).

Here, Netlist was unequivocal about the disputed language's meaning. In the same filing in which Netlist amended the claims, Netlist repeatedly distinguished prior art because the art lacked a logic element that generates recited output signals by responding to all four enumerated signals. For example, Netlist acknowledged that Amidi discloses an element that generates "control signals" "based on the row address signals and chip-select signals," i.e., enumerated signals (i) and (iii). Appx16808. It explained that Amidi's element still differed from the claimed logic element because "Amidi's CPLD 604 never receives bank address signals and hence Amidi's control signals cannot be generated based on bank address signals." Appx16808. Netlist stated that "Amidi is further deficient" because it fails to disclose "the CPLD generating the gated CAS signals or chip-select signals in response to the *PLL clock signal*." Appx16808 (emphasis in original). Netlist also stated that "Amidi provides no recognition to use both the bank address signals and a row address signal for rank multiplication or the generation of chip-select signals or CAS signal[s]." Appx16810; Appx16809, Appx16811 (similar).

Thus, Netlist distinguished the prior art for failing to disclose a logic element that generates required output signals in response to all four signals (i)-(iv). Appx16808. Even were the claim text ambiguous, Netlist's unambiguous statements would be enough to disclaim an interpretation that allows generating the recited output signals in response to less than all four enumerated signals. *See Krippelz*, 667 F.3d at 1266-67 (relying on unambiguous prosecution statements from reexamination to find disclaimer). Regardless, Netlist's prosecution statements reinforce the claims' text.

c. Google and Inphi ignore the claims' text and the intrinsic record

Google and Inphi are wrong that the words "in response at least in part" in claim 1 mean that the claims cover a logic element that responds to any one of the four enumerated signals.

For one, Google and Inphi concede that all challenged claims must be interpreted identically on this issue, just as they did before the Board. Google Br. v-vi; Inphi Br. 11-12; Appx16872-16873; Appx16901-16909. That dooms their reliance on the words "in part" in claim 1 because more than half of the challenged independent claims omit those words. Independent claim 52, among others, recites a logic element that "responds to at least" the four enumerated signals. Appx16782-16783; Appx16787-16789 (claim 67); Appx16790-16792 (claim 77); Appx16793-16794 (claim 82); Appx16795-16797 (claim 87). By conceding that claims both

with and without "in part" should be interpreted similarly on the disputed issue, Google and Inphi concede that the "in part" language cannot carry the weight they place on it.

For that reason, Google and Inphi are wrong that the Board "disregarded" claim language because it sometimes omitted "at least in part." *Contra* Google Br. 43; Inphi Br. 30. Unlike Google and Inphi, the Board understood it was interpreting and applying multiple independent claims with varying claim language. Appx121-122 (discussing claim 52). The Board thus reasonably used language common to all claims when evaluating the "logic element" limitation. And as explained, the Board's construction gives meaning to "at least" and "at least in part" because those phrases indicate that, although the logic element must generate the specified output signals by responding to all four enumerated signals, the logic element may also generate the specified output signals by responding to additional signals. *Supra* p. 32. And although unnecessary to the dispute here given Google's and Inphi's concession, the Board also gave separate meaning to "in part"—it explained that "in part" requires "that the signals that enter logic element 40 have some purpose and affect the output signals." Appx88-91 (each input signal must be "used in some manner, whether directly or indirectly, to generate the" recited output signal; used "in some fashion").

Google also is wrong (at 43-44) in arguing that the open-ended transition "comprising" affects the meaning of the "logic element" limitation. "'Comprising' is not a weasel word with which to abrogate claim limitations." *Spectrum Int'l v. Sterilite,* 164 F.3d 1372, 1380 (Fed. Cir. 1998). "Comprising" affects claim scope as a whole; it "does not reach into each [claim element] to render every word or phrase therein open-ended." *Dippin' Dots v. Mosey*, 476 F.3d 1337, 1343 (Fed. Cir. 2007). And "comprising" in a claim's preamble cannot be used to "frustrate the plain meaning" of an element in the claim's body. *Wis. Alumni Research Found. v. Apple*, 905 F.3d 1341, 1348 n.8 (Fed. Cir. 2018).

The inference Google tries to draw from "comprising" is implausible anyway. Google argues that if "at least in part" means, as it plainly does, that the logic element must respond to all four enumerated signals but also may respond to additional signals, that "would render 'at least in part' meaningless" because "comprising" "already permits taking into account additional signals." Google Br. 43-45. Not so. If the claims omitted "at least in part" and were interpreted as meaning a logic element that responds to only the four enumerated signals, "comprising" would not change the requirement for a logic element that responds to only those four signals. *Dippin'*, 476 F.3d at 1343. Netlist added the modifiers "at least" and "at least in part" to remove any ambiguity about whether other signals were permitted, which is what Google itself argues patent owners are supposed to do when amending claims

during reexamination. Google Br. 42, 45; *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004).

Unable to reconcile the claims' text with their desired interpretation, Google and Inphi try to paint the '912 patent specification as inconsistent with the text. That argument fails because "[w]hen claim language has as plain a meaning on an issue as the language does here, leaving no genuine uncertainties on interpretive questions relevant to the case, it is particularly difficult to conclude that the specification reasonably supports a different meaning." *Straight Path*, 806 F.3d at 1361.

Google and Inphi are wrong about the specification anyway. Google again pins its argument on the term "density transition bit," wrongly arguing that nothing in the specification supports "requir[ing] that both the claimed 'at least one row address signal (signal i) and 'the bank address signals' (signal ii) simultaneously serve as density transition bits." Google Br. 45-47; *supra* pp. 28. Google failed to preserve this issue, as the Board found, because it failed to "present a separate argument that the 'logic element limitation lacks written description support if construed in [the] conjunctive." Appx163. Regardless, neither the "logic element" limitation's plain text nor the Board's construction refer to a density transition bit or limit the claims based on which signals serve as density transition bits. Nothing about "density transition bits" thus affects the meaning of the disputed limitation.

Google argues otherwise by misstating what the patent means by "density transition bits," arguing it means any "signal(s) used to generate the claimed output." Google Br. 4. The patent uses that term more narrowly to refer to the "signal bit which is used to access the additional memory," which depends on how memory locations are organized within a memory device. Appx223-224 (col.12:21-col.14:23 and Tables 3A, 3B, 4). And the patent teaches that the logic element responds to more than just density transition bits to generate output control signals. For example, the patent consistently shows a logic element generating the required output signals by responding to chip-select signals even though these signals are not density transition bits. *E.g.*, Appx200-201, Appx204 (Figures 1A, 1B, 3A, 3B), Appx221-222 (Tables 1, 2). For that reason, Google is wrong that both the row address signal and the bank address signals must be density transition bits under the Board's construction. Hence, Google's repeated arguments about whether row address and bank address signals can "simultaneously serve" as density transition bits proves nothing.

Equally unavailing is Inphi's argument that the tables in the patent support interpreting "logic element" as broadly requiring responding to any one of the enumerated signals. Inphi Br. 31-35. For one, Inphi is wrong in assuming that the tables list all input signals to which the logic element responds; the specification identifies embodiments that produce output control signals by responding to clock

signals and bank address signals even though no table lists those signals. Appx222 (col.9:18-21); *supra* pp. 33-34.

Inphi also is wrong about what the tables show. Table 1 provides one example of logic states for output chip-select signals based on certain inputs:

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Appx221. Inphi argues that because Table 1 and Table 2 show some states in which input signals are marked with an "x" as "don't care"—meaning for the specific state the output is the same regardless of the value of that particular input—"not all of the signals need to be utilized at the same time." Inphi Br. 32-35. That argument proves nothing, because nothing in the Board's decisions turn on whether a logic element utilizes signals "at the same time." Appx1-166. In any event, by requiring a logic element that responds to all four enumerated signals, the claims cover a logic element that responds to all four enumerated signals "at least some of the time." *Broadcom. v. Emulex*, 732 F.3d 1325, 1333 (Fed. Cir. 2013). Thus even under Inphi's mistaken reading of the record, the tables are consistent with the claims' text.

Both Google and Inphi also insist without support that the patent's figures, such as Figures 1A and 1B, "lack any features that could be read as requiring signals (i)-(iv)." Inphi Br. 34; Google Br. 45-47. Neither party explains why these figures depict a logic element receiving all four enumerated signals as input. Given the claims' text and the patent's description, the only reasonable reading of the figures is that the logic element receives all enumerated signals as input because it responds to those signals to generate the output. Appx200-201; Appx220-222 (col.5:28-col.9:18-21); Appx88-91 (Board reasoning similarly); *supra* pp. 32-34.

In the end, Inphi gives up the game by conceding that the claims "require[] that the logic element generates the gated CAS or chip-select signals in response to 'the at least one row address signal' and 'the at least one chip-select signal.'" Inphi Br. 34. Google is never as forthright, but also appears to concede that the logic element must respond to those signals, repeatedly framing its arguments only as whether the logic element can respond to "*either* extra row address *or* bank address signals." Google Br. 41-47. But nothing in the claims' text suggests any reason for requiring that the logic element respond to chip-select signals and the row-address signal but not the bank address signals. Instead, the claims require the logic element respond to the chip-select and row-address signals *only because* they require the logic element respond to all four enumerated signals. Appx16758-16797.

The Board correctly gave the claims their plain meaning, which is the broadest reasonable meaning the intrinsic record supports.

B. Substantial Evidence Supports The Board's Findings Underlying Non-Obviousness

Under the Board's adopted construction, Google and Inphi present one-sided versions of the evidence for the unpatentability grounds each pressed below—obviousness based on Amidi, Dell 2, and related references for Inphi, and obviousness based on Micron, Amidi, and related references for Google. Both ask this Court to weigh their versions of the evidence in the first instance and find for them. "[A]s an appellate court, it is beyond [this Court's] role to reweigh the evidence or consider what the record might have supported." *Apple v. Samsung Elecs.*, 839 F.3d 1034, 1062 (Fed. Cir. 2016) (en banc). The Court should reject these factual challenges.

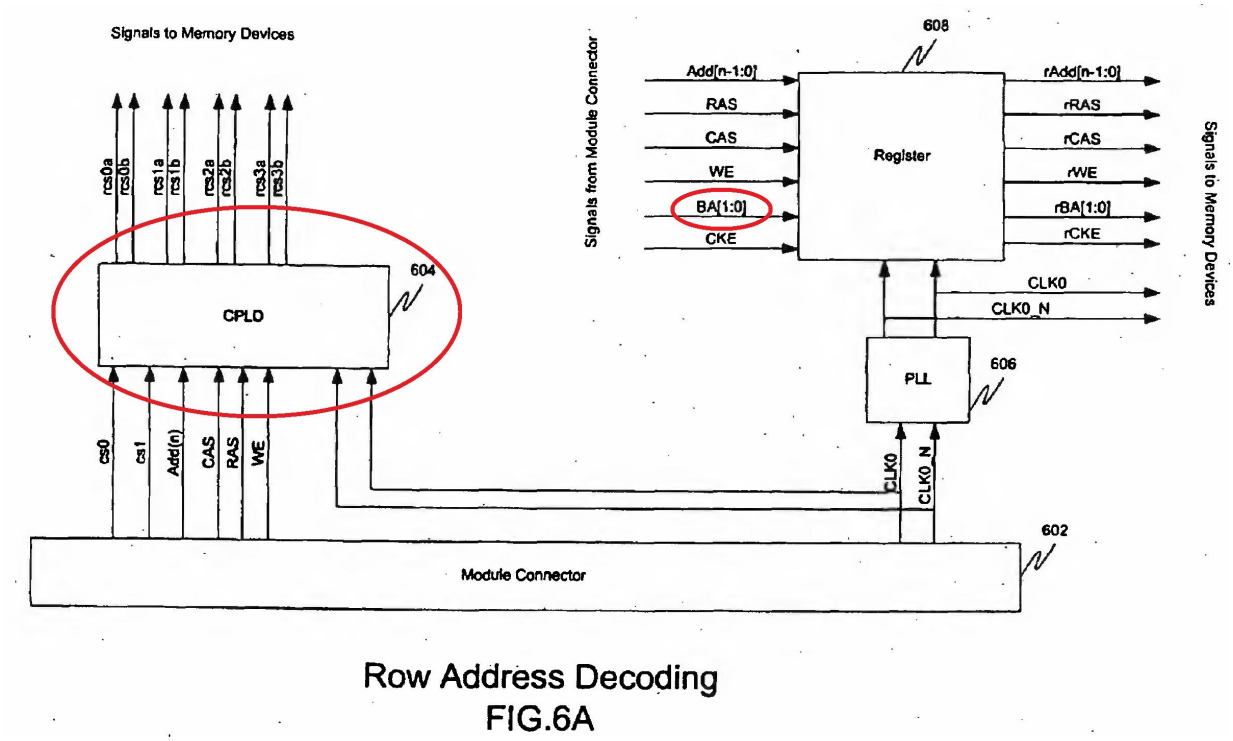
1. On Inphi's appeal, substantial evidence supports that Amidi, Dell 2, and related references fail to teach or suggest the "logic element" limitation

a. Ample evidence supports the Board's findings

Amidi's and Dell 2's disclosures, and expert testimony, support the Board's finding that Amidi and Dell 2 fail to teach or suggest the disputed logic element limitation. Appx120-130.

As Inphi never disputes, neither Amidi nor Dell 2 teaches a logic element generating chip-select or gated column access strobe signals in response to at least

the four enumerated signals: a row address signal, bank address signals, at least one input chip-select signal, and a PLL clock signal. Inphi Br. 36-46. Amidi's Fig. 6A, shown below, discloses a Complex Programmable Logic Device (CPLD) 604, which Inphi argues "correspond[s] to the claimed 'logic element'" (Br. 15):



Row Address Decoding
FIG.6A

Appx438 (markup added), Appx445. As the figure shows and the Board repeatedly found, Amidi's CPLD receives no bank address signals (BA[1:0]). Appx23, Appx39-42, Appx124; Appx438, Appx445. Nor does the CPLD receive a PLL clock signal from the memory module PLL; Amidi indicates that PLL 606's generated clock signal is never transmitted to the CPLD. Appx438, Appx445. Amidi's CPLD thus differs from the claimed logic element at least because its CPLD never generates an output signal in response to either bank address signals or a PLL

clock signal; it never even receives these signals as inputs. Appx438; Appx16821-16822, Appx16816-16855.[1]

Nothing in Dell 2 bridges the gap between Amidi and the claims. Inphi concedes that "Dell 2 focuses on remapping address signals to support additional banks as opposed to ranks" (Br. 15-16):

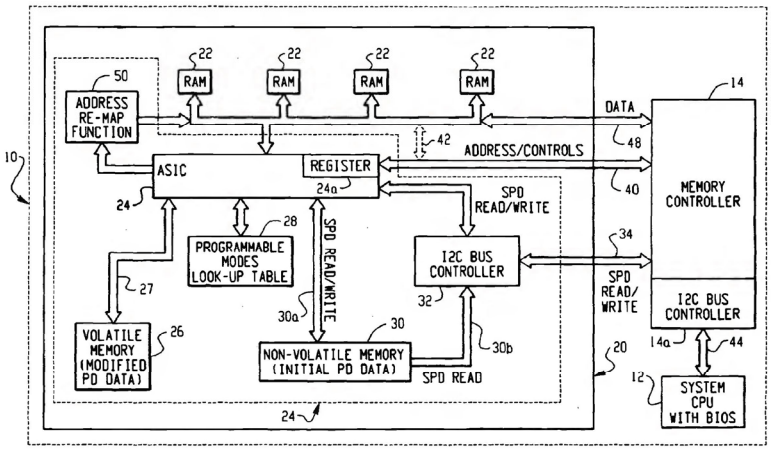


Fig. 1

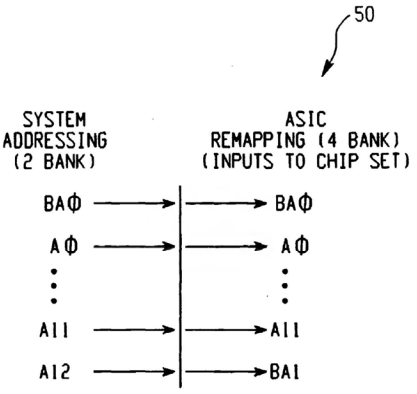


Fig. 1A

Appx2301-2302; Appx126; Appx930; Appx943; Appx6682-6683, Appx6678-6706; Appx16824. Dell 2 teaches to perform this remapping "by a simple switch circuit" that "connect[s] the highest order address signal" to "the BA1 [bank address] input pin of the memory devices." Appx2302; Appx2307 (col.8:29-43). As the Board found in both its first and second decisions, Dell 2 describes no circuitry for

[1] The Board also rejected that register 608 satisfies the claimed logic element limitation. Appx123, Appx128. Inphi's opening briefing fails to challenge that finding and so forfeits the issue. Inphi Br. 14, 36-46; *SmithKline Beecham v. Apotex*, 439 F.3d 1312, 1319 (Fed. Cir. 2006).

generating chip-select or gated column access strobe signals. Appx83-84; Appx126-128; Appx2301-2302; Appx2307 (col.8:29-43).

Substantial evidence also supports the Board's finding that no evidence suggests combining Amidi and Dell 2 to arrive at the claimed "logic element" limitation. Appx124-129. Based on the above evidence, the Board found that Dell 2 would have suggested "using a logic element, like Amidi's CPLD, to generate a control signal in response to a bank address signal for navigating to the correct *bank*." Appx126-127 (emphasis by Board); Appx2302; Appx2304 (col.2:32-37, 49-51), Appx2307 (col.8:20-40). But the Board found no evidence for "why one skilled in the art would have recognized a CPLD, like Amidi's, generates *chip-select* signals in response to bank address signals and the other recited signals." Appx126 (parenthetical omitted). Netlist's expert's opinion, which the Board quoted, supports that finding: "'[t]here is no disclosure or suggestion [in Dell 2] of using [a] bank address to generate a control signal, such as a chip-select signal or a CAS signal.'" Appx127 (quoting Appx16824; alterations by Board). The expert similarly opined that no evidence "suggest[s] to repurpose a bank address signal for rank multiplication purposes," meaning to generate the type of output signals required by Netlist's claims. Appx16824; Appx127 (Board crediting same).

The Board found a similar lack of evidence for combining Amidi and Dell 2 to generate gated column access strobe signals (rather than chip-select signals) in

response to the four enumerated signals. Appx128-129. Amidi lacks any disclosure for using logic on a memory module to generate new column access strobe signals. Appx128; Appx438, Appx445. And although Dell 2 may suggest "storing a bank address signal for use with a logic element (e.g., ASIC 24) during CAS time," no evidence suggests "generat[ing] a CAS signal in response to a bank address signal," nor in response to multiple bank address signals, a chip-select signal, and the other signals recited in the claims. Appx83-84, Appx128. The Board again credited Netlist's expert while finding Inphi's expert not "persuasive in teaching or suggesting" the claimed "logic element" limitation. Appx83-84, Appx128-129 (citing Appx27413-27421, Appx27410-27424; Appx16824).

Given the utter lack of evidence, the Board correctly held Amidi and Dell 2 fail to render the claims obvious.

b. None of Inphi's conclusory arguments shows error

i. Inphi reargues the facts

Although Inphi insists that the Board erred as a "as a matter of law," it really just reargues the facts. Inphi Br. 36-46. None of Inphi's arguments shows the Board lacked substantial-evidence support or otherwise erred.

First, Inphi is wrong that the Board failed to account for the "inferences and creative steps" a skilled artisan would have followed based on Amidi and Dell 2. Inphi Br. 36-42. Inphi's own brief shows the opposite—it repeatedly cites to the

"First Board" as having performed the proper analysis while arguing the "Second Board" did not. Inphi Br. 36-42. The "First Board" and the "Second Board" are the exact same Board, composed of the exact same panel members. Appx4, Appx111. Indeed, the same judge authored both decisions. Appx4, Appx111. And the Board did not start from scratch in authoring the second decision; it built on its earlier decision, repeatedly citing to and relying on that decision. *E.g.*, Appx122-129. Inphi thus implicitly concedes that the Board's analysis was legally proper by conceding that the analysis from the Board's first decision was so; the Board applied the same legal analysis in both.

Nor did the Board "require[e] that Dell 2's bank expansion process be bodily incorporated into Amidi." *Contra* Inphi Br. 41. The Board acknowledged that Dell 2 suggested modifying Amidi to respond to a bank address signal "to generate signals for *bank* selection." Appx126-127 (emphasis by Board). It found no evidence suggested such a modification would have involved generating chip-select or column access strobe signals in response to the bank address signal, let alone multiple bank address signals and all the other signals required by the claims. Appx126-129. The Board repeatedly considered what the prior art "collectively" would have taught, which is the exact analysis Inphi says is required. Appx122-129; Inphi Br. 41-42; *see KSR Int'l v. Teleflex*, 550 U.S. 398, 418 (2007); *In re Keller*, 642 F.2d 413, 424-25 (C.C.P.A. 1981); Appx143 (Board citing and applying *KSR*).

Second, Inphi cites no support for its bald assertion that the claims would have been obvious "[b]ecause increasing memory capacity inherently includes increasing the number of bank address signals." Inphi Br. 42-46. In fact, the '912 patent shows that memory capacity often increases without increasing the number of bank address signals: DDR1 memory devices with capacities ranging from 128 Mb to 1 Gb all use 4 banks and thus have the same number of bank address signals; DDR2 memory devices with capacities of 256 and 512 Mb also use 4 banks, while devices with capacities from 1 to 4 Gb use 8 banks. Appx223-224. The Board was not required to credit Inphi's unsupported attorney argument which, in any event, the record directly contradicts. *Invitrogen v. Clontech Labs.*, 429 F.3d 1052, 1068 (Fed. Cir. 2005).

Third, Inphi repeatedly relies (Br. 44-46) on its employee Dr. Wang's opinions but fails to grapple with the Board's findings that Dr. Wang's opinions were not "persuasive" nor "probative" because "there is no evidence to support" them. Appx83; Appx128 (citing Appx27413-27421). Inphi never acknowledges the Board's findings but appears to recognize the problem because it avoids citing the third Wang declaration—the most recent declaration and the one the Board cited—and instead cites only to the older second declaration. Inphi Br. 44-46 (citing and quoting Appx23037-23039). There is no material difference between the two; both offer conclusory and unsupported opinions about what would have "been apparent"

and was allegedly "widely known" to skilled artisans. *Compare* Appx23037-23039, Appx23035-23041, *with* Appx27413-27421. Because Inphi fails to acknowledge the Board's refusal to credit Dr. Wang's testimony, it fails to show any error in that finding and has forfeited any such challenge. *SmithKline*, 439 F.3d at 1320 ("arguments not raised in the opening brief are waived"). Nor could Inphi show any error. The Board's unchallenged determination to credit opinion evidence from Netlist's expert over Inphi's employee "'is the special province of the trier of fact.'" *Elbit,* 881 F.3d at 1358.

Fourth, besides Dr. Wang's unpersuasive testimony, Inphi has nothing but attorney argument to support its insistence that skilled artisans "would have had ample motivations to make necessary design choice modifications" to Amidi and Dell 2 to arrive at the claimed inventions. Inphi Br. 43-46. Unlike the Board, which cited and explained how each reference supported its finding, Inphi's arguments are untethered from any such record evidence. The Board rightly rejected those arguments because "[u]nsubstantiated attorney argument regarding the meaning of technical evidence is no substitute for competent, substantiated expert testimony." *Invitrogen*, 429 F.3d at 1068. And even if Inphi had such evidence, that still would fail to show an absence of evidence supporting the Board. After all, the question is not whether the Board could have reasonably concluded differently, but whether no reasonable factfinder could have found as the Board did. *Gartside*, 203 F.3d at 1312.

ii. Inphi concedes that JEDEC 21C adds nothing relevant to the dispute here

Inphi's challenge based on Amidi, Dell 2, and JEDEC 21C falls with its failed challenge based on Amidi and Dell 2. Appx130-131. Inphi concedes this, arguing only that "[f]or the reasons given" in its arguments about Amidi and Dell 2 the Court should "reverse the Second Board's withdrawal of the Examiner's adoption of the new ground of rejection" based on Amidi, Dell 2, and JEDEC 21C. Inphi Br. 47-48. Because the Board correctly found the claims patentable over Amidi and Dell 2, it correctly found them patentable over Amidi, Dell 2, and JEDEC 21C.

iii. Inphi's proposed new ground of rejection is procedurally and substantively defective

Inphi makes a last-ditch attempt to raise a new ground of rejection based on Amidi, Dell 2, and JEDEC 21C for original claims 16 and 17. Inphi Br. 48-49. Because Inphi never proposed this rejection to the Board, it is too late for Inphi to raise it now. *In re Margolis*, 785 F.2d 1029, 1032 (Fed. Cir. 1986). Nor could Inphi have proposed this rejection to the Board because Netlist never amended these claims—after requesting reexamination, requesters may propose new grounds of rejection only "where such new proposed rejection is necessitated by patent owner's amendment." Manual of Patent Examining Procedure § 2666 (citing 37 C.F.R. § 1.948(a)(2)).

Even so, Inphi fails to show the Board erred on claims 16 and 17. Inphi tries to bootstrap an alleged error on claims 132 and 133 into an error on claims 16 and 17. Inphi Br. 48-49. But Inphi admits (Br. 49) that claims 16 and 17 lack the logic element limitation, which is the only basis for error on claims 132 and 133 that Inphi alleges. Thus, even were the Court to hold the Board erred on claims 132 and 133, the Board's decision on claims 16 and 17 would independently stand.

2. On Google's appeal, substantial evidence supports the Board's finding that Micron, Amidi, and related references fail to teach or suggest the claimed "logic element"

a. Ample evidence supports the Board's findings

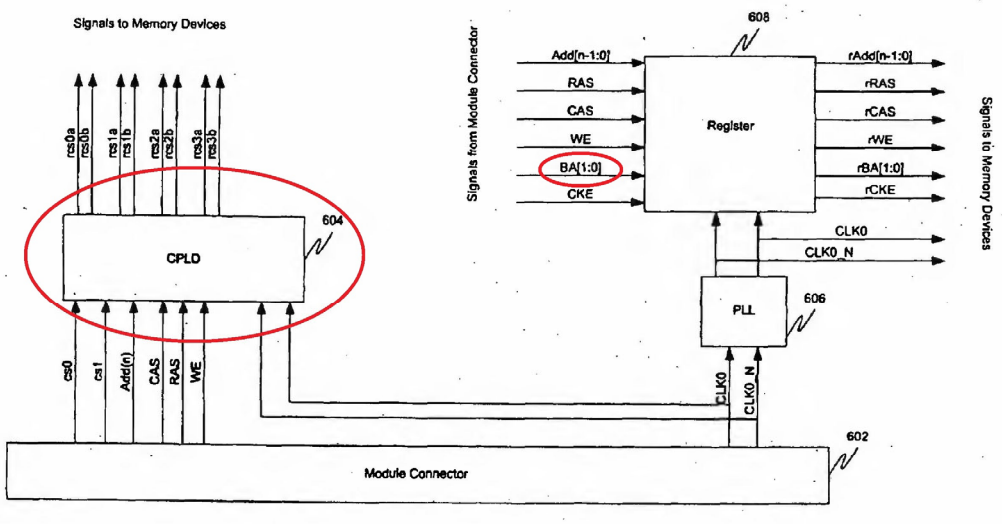
In arguing obviousness based on Micron and Amidi, Google bases its argument almost entirely on Amidi. Google Br. 49-58. It cites to Micron just once as an additional "*see also*" cite. Google Br. 53. Yet as already explained and as the Board found, Amidi teaches logic elements that differ from the claimed logic element. Appx133; *supra* pp. 43-45. Amidi discloses a logic device for generating chip-select signals but never teaches that logic device receiving bank address signals or a PLL clock signal to generate those chip-select signals. Appx438, Appx445. And Amidi never discloses a logic element for generating column access strobe signals, nor did Google argue otherwise; the Board found both Google and its expert "focus[] on generating chip-select signals." Appx144; Appx438, Appx445.

The Board rightly rejected on the facts two additional obviousness theories that Google put forth, and substantial evidence supports those findings. Appx133-144. First, despite agreeing that Amidi and background knowledge suggest a logic element can generate a chip-select signal in response to "*a* free signal," the Board found that evidence does not suggest the claimed logic element, which must generate the required output in response to multiple bank address signals *and* a row address signal regardless of whether those are "free" signals. Appx135-137 (emphasis by Board) (citing Appx97-98). As the Board found, Amidi itself supports that conclusion—it teaches using an extra row/column address bit for rank expansion, and the Board found that a skilled artisan would have understood that in some circumstances a free single bank address bit could serve a similar purpose. Appx135-136; Appx438, Appx445. Nothing in Amidi suggests any reason for using multiple bank address signals, nor renders obvious using such signals together with the other enumerated signals. Appx135-137; Appx438, Appx445.

The portions of Google's expert opinion on which the Board relied similarly support that finding. Appx135-137 (citing Appx455-456; Appx4337-4339); Appx49-456. The expert focuses on a reason for responding to a single bank address bit without suggesting any reason for more. Appx455-456; Appx4337-4339, Appx4329-4339. He states that, for the type of memory described in Amidi, a skilled artisan would understand that a logic element using bank address signals "is not

necessary for any purpose" because the bank address signal "bits are not used for address signal conversion." Appx455-456. The expert identified one exception, where a single extra "bit of the bank address field must be processed by the logic" because the system controller sends a bank address field with one extra bit. Appx455-456; Appx4337-4339. Nothing in that explanation identifies any reason for a logic element to generate the required output in response to multiple bank address signals, nor multiple bank address signals together with a row address signal. Appx455-456; Appx4337-4339.

Second, the Board rightly rejected Google's theory that Amidi inherently discloses a logic element generating the required output in response to bank address signals and a row address signal. Appx137-144. The Board found Google failed to show by a preponderance of the evidence that using multiple bank address signals is "necessary" to generate chip-select output signals as taught by Amidi. Appx137-144 (quoting Google). Again, both Amidi itself and Google's own expert support the Board's finding. Amidi includes detailed diagrams showing the input signals for generating chip-select signals. Appx438-441. During both row and column address decoding, Amidi shows the complex programmable logic device (604) generates chip-select signals without receiving bank address signals:



Row Address Decoding
FIG.6A

Appx438-441. Amidi shows sending bank address signals (BA[1:0]) to a register for storing and delivering to the memory devices, but never shows routing those signals as inputs to the logic device. Appx438-441; Appx445 (¶50) (describing different signals sent to CPLD and register). Thus as the Board found, Amidi shows that bank address signals are unnecessary for a logic element that generates output chip-select signals, contradicting Google. Appx137-138.

Statements from both Google's and Netlist's experts support the same conclusion. Google's expert explained that Amidi's logic "element does not use the bank address field as an input," and the bank address "bits are not used for address signal conversion." Appx454-455. "A person of ordinary skill in the art may still choose to route the bank address field of the DDR-1 devices as an input to the conversion logic, but it is not necessary for any purpose." Appx455-456; Appx2287 (similarly testifying that "Amidi correctly identifies that the bank address signals are

not needed to generate any output control signals"). Netlist's expert similarly explained that "Amidi discloses the internal circuitry of the CPLD—which does not utilize any bank address signals." Appx16822-16823. Instead, "Amidi discloses that the register receives the bank address signals so that they can be passed through to the DDR memory devices." Appx16823; *see* Appx929; Appx6682 (similar). The Board correctly relied on this evidence in finding that the asserted prior art neither teaches nor renders obvious claims to a logic element generating the required output signals in response to bank address signals, a row address signal, and the other enumerated input signals. Appx138-139, Appx142-143 (citing same expert statements).

b. None of Google's arguments shows reversible error

Rather than show how Micron or Amidi discloses or renders obvious claims reciting the "logic element" limitation, Google relies on yet more prior-art references: Dell 2, JEDEC 79C, and Olarig. None of these references discloses or suggests the disputed limitation either.

Google argues these references all apiece. Br. 49-58. But before the Board they formed separate alleged grounds of unpatentability: Micron, Amidi, Dell 2, and JEDEC 79C for one set of claims, and Micron, Amidi, and Olarig for another set. Appx147-148 (Board identifying claims). If Google now is suggesting combining references or claims differently, "it is inappropriate for this court to consider

rejections that had not been considered by or relied upon by the Board." *Margolis*, 785 F.2d at 1032.

i. Google doubly forfeited its challenge based on JEDEC 79C

As an initial matter, Google's arguments based on JEDEC 79C (Br. 53-54) are doubly barred. The Board held that "[r]egarding JEDEC 79C, Requester 3 [Google] does not explain how this reference is being relied upon in its Appeal Brief." Appx149. The Board held Google also failed to address JEDEC 79C in its earlier "cited comments, submitted August 29, 2011." Appx149. The Board "thus determine[d] Requester 3 has not sufficiently demonstrated how JEDEC 79C teaches or suggests the claimed features missing from Micron, Amidi, and Dell 2." Appx149. There thus is no issue for this Court to review on JEDEC 79C because the Board declined to consider the issue after Google failed to develop it and this Court refuses to consider issues "not meaningfully raised" before. *Apple*, 839 F.3d at 1062. That is especially true when, as here, the Court reviews an agency decision on factual issues like the scope and content of the prior art, because the Court must judge the agency based on the grounds the agency reached. *In re Zurko*, 258 F.3d 1379, 1385-86 (Fed. Cir. 2001); *SEC v. Chenery*, 318 U.S. 80, 87 (1943). It thus "would be inappropriate for [the Court] to consider references not relied upon by the Board." *Zurko*, 258 F.3d at 1386 n.2.

Additionally, Google's opening appeal brief never challenges, or even acknowledges, the Board's determination that Google failed to preserve reliance on JEDEC 79C. Google Br. 1-58. Google thus forfeited any challenge to that determination. *SmithKline*, 439 F.3d at 1319 ("arguments not raised in the opening brief are waived").

Because Google forfeited reliance on JEDEC 79C before the Board, the Board so found, and Google fails to challenge that finding on appeal, the Court should not consider the issue.

ii. Nothing in Dell 2 or JEDEC 79C overcomes Micron's and Amidi's deficiencies

Even if Google could rely on JEDEC 79C, Google's arguments about Dell 2 and JEDEC 79C fail to show the Board erred. In arguing about these references, Google conflates logic for generating an output bank address signal with the claimed logic for generating chip-select signals. Google Br. 49-55. Google argues that "the input bank address signals are needed to select a previously stored address signal at column access time." Google Br. 49-55. As alleged support, Google relies on Dell 2's disclosure of "address remapping" to generate a bank address signal and what Dell 2 allegedly teaches doing "'to ensure the correct bank is addressed.'" Br. 50-52 (quoting Appx127); *supra* pp. 45-47 (discussing Dell 2). Google cites no evidence for why alleged teachings about generating a bank address signal in response to another bank address signal apply to generating chip-select signals, the

only claimed output signals Google addressed at the Board. Google Br. 49-55; Appx144. As Google concedes, bank address signals address different memory banks within an individual memory device; chip-select signals select between different groups (ranks) of memory devices themselves. Google Br. 5-9. Google elides the difference between the two without acknowledging it or explaining the gap. Google Br. 49-55.

Google's forfeited argument based on JEDEC 79C about "interleaving" commands to different memory banks fails for similar reasons. Google Br. 53-55. Google argues that because JEDEC 79C shows interleaving (i.e., alternating) the commands between different banks, the logic element "needs some mechanism to keep track of which stored signals belong to which banks." Google Br. 54. But Google never cites anything from JEDEC 79C disclosing such a need, never identifies what "some mechanism" would be, and never explains how "some mechanism" relates to the requirement for a logic element that generates output chip-select signals in response to a row address signal, bank address signals, input chip-select signal(s), and a PLL clock signal. Google Br. 53-55. Thus, had Google presented this issue to the Board, the Board would have rightly rejected it for leaving unexplained differences between the prior art and the claimed logic element limitation. *See* Appx138-140 (Board dismissing expert testimony for this reason).

Google also has no answer to the Board's finding that Amidi contradicts Google's inherency theory, that "input bank address signals are needed" (Br. 54-55) to generate output chip-select signals. Appx137-138. As explained (*supra* pp. 43-45), Amidi shows detailed circuit diagrams that send bank address signals to, for example, a register but never as inputs to its complex programmable logic device. Appx438-441; Appx445 (¶50). Amidi thus shows using its logic device to generate chip-select output signals without the input bank address signals that Google argues are needed. Appx137-138.

iii. Nothing in Olarig overcomes Micron's and Amidi's deficiencies

Google also argues (Br. 52-54) that the Board erred in finding that the combination of Micron, Amidi, and Olarig would not have suggested the claimed logic element limitation. Netlist's unrebutted expert declaration alone supports the Board's rejection of that argument and requires affirmance on this issue. The Board credited Dr. Sechen's conclusion that "Amidi and Olarig alone or in combination with Micron do not suggest generating gated CAS, chip-select, or rank-selecting signals in response to both a row address signal (i.e., signal (i)) and bank address signals (i.e., signals (ii)) as well as signals (iii) and (iv)." Appx147 (citing Appx16828-16830). As Dr. Sechen explained "Olarig is an asynchronous EDO memory that does not include a chip-select signal at all, and would be incompatible with a synchronous system using a PLL." Appx16830. In addition "Amidi does not

use bank addresses at all for generating chip-select signals." Appx16830. The Board found that Google "provide[d] no rebuttal to Dr. Sechen's testimony." Appx147. These unrebutted statements alone support the Board's decision and require affirmance.

Even without Dr. Sechen's unrebutted declaration, the Board reasonably found that Olarig alone or combined with Micron and Amidi would not have suggested the claimed logic element limitation. Appx144-147. Olarig involves translating between memory devices supporting multiple banks and memory devices without banks:

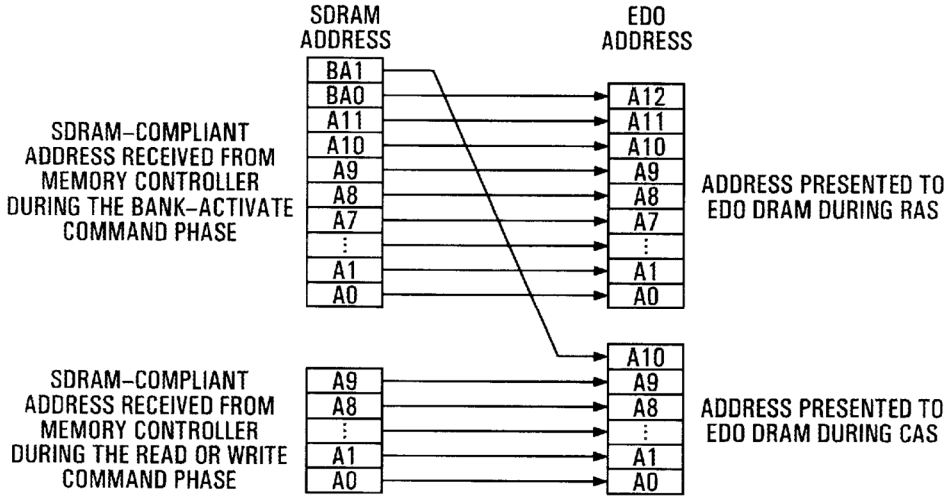


FIG. 6

Appx7402; Appx7418 (col.22:3-58); Appx16829-16830 (Dr. Sechen explaining Olarig). As shown, Olarig discloses remapping one bank select address (BA0) as a row address signal (A12 "during RAS," meaning row address strobe), and the other

(BA1) as a column address signal (A10 "during CAS" meaning column address strobe). Appx7402; Appx7418 (col.22:3-58). To use the bank address signal BA1 during the column address strobe, Olarig teaches that BA1 should be "latched internally," meaning stored, for later use. Appx7418 (col.22:3-58).

As the Board found, nothing in Olarig supplies what Micron and Amidi lack—any reason for a logic element to "generat[e] a control signal, such as a chip-select signal, in response to both at least one row address signal (e.g., recited signal (i)) and bank address *signals* (i.e., signals (ii))." Appx145-146 (emphasis by Board). Because Olarig simply remaps one bank address signal to one row or one column address signal, it never suggests generating an output signal in response to more than one input signal, nor to different types of input signals. Appx7402; Appx7418 (col.22:3-58).

For the first time on appeal, Google makes a distinctly new factual argument about Olarig, that Olarig and alleged background knowledge of bank address interleaving would have suggested the claimed logic element limitation. Google never presented that issue to the Board, so it is "beyond" the Court's "role" to consider the issue now. *Apple*, 839 F.3d at 1062. And even without that, Google ignores Olarig's express disclosures. Olarig mentions that newer memory devices with banks allow interleaving "[t]o reduce the need for wait states" when accessing "adjacent memory locations." Appx7408 (col.2:12-29). It states that to implement

address remapping, which allows computer systems to support older memory devices without banks, the memory controller "must reduce the rate of back to back cycles as well as increase the latency between adjacent memory cycles by inserting dummy or idle states." Appx7419 (col.23:18-55). Olarig thus explains that address remapping conflicts with interleaving. It does not suggest, as Google now argues, combining the two.

iv. The Board reasonably resolved the battle of the experts

Google fails to fill the voids in the prior art with hindsight-driven statements from its expert that the Board found other evidence contradicts, including the expert's own statements. Google Br. 52-57.

After Netlist began narrowing its claims, Google's expert argued without corroboration that a chip designer "will use the chip select and bank address signals provided by the memory controller to select one of the eight pairs of banks in the rank-multiplying module." Appx4336. Nothing about that statement required the Board to find that the prior art would have rendered obvious claims reciting the logic element limitation. For one, the expert's statement was actually about "select[ing] one of the eight pairs of banks." Appx4336; Appx4335-4337 (also arguing about "[t]he obvious way to know which of the two banks" to select). The claims recite something different, a logic element that generates *chip-select* signals in response to bank address signals, a row address signal, and the other signals. Appx16758-16797.

Chip-select signals select among ranks, or groups, of memory devices, not banks of memory within a memory device. Google Br. 5-9. As the Board explained in detail, Google's expert failed to explain what was obvious about generating chip-select signals in response to bank address signals. Appx138-140 (citing and discussing Appx4335-4337; Appx7388-7393); Appx7385-7395. Thus, even accepting the expert's unsupported statements, which the Board was not required to do, nothing in those statements contradicts the Board's findings that the prior art neither discloses nor suggests the claimed logic element. Appx138-140 (Board making similar point).

In any event, the Board had good reasons for rejecting the expert's post-hoc rationales about what would have been obvious. As the Board recognized (Appx140-141), before making the above statements the expert had already stated that "Amidi correctly identifies that the bank address signals are not needed to generate any output control signals" and that the "bank address field of the DDR-1 devices as input to the conversion logic" is "not necessary for any purpose." Appx454-456; Appx2287. Given this earlier testimony, the Board reasonably refused to credit the expert's later uncorroborated statements about what allegedly would have been obvious. *TQ Delta v. Cisco Sys.*, 942 F.3d 1352, 1359-61 (Fed. Cir. 2019) (this Court "reject[s] obviousness determinations based on conclusory and unsupported expert testimony").

Google is wrong that the Board "misinterpreted" its expert's statements. *Contra* Google Br. 56-57. As already shown, the expert was unambiguous that Amidi's logic "element does not use the bank address field as input," that bank address "bits are not used for address signal conversion," and that "Amidi correctly identifies that the bank address signals are not needed to generate any output control signals." Appx454-456; Appx2287. Google ignores all except the last statement, while trying to qualify the last as being about what Google calls the "first case" rather than the "second case." Google Br. 56-57. Google's expert directly contradicts Google—he explained that Amidi "provides as an example of the case where the memory devices used in the lower cost module have the same number of banks as the memory devices in the originally specified module," what Google calls the "first case." Appx2287. And he explained that "Dell [2] provides as an example the case where the memory devices used in the lower cost module have a larger number of banks than the memory devices in the originally specified module," what Google calls the "second case." Appx2287. But the expert's opinion was that, for *both* cases, "Amidi" and "Dell" "correctly identif[y] that the bank address signals are not needed to generate any output control signals for the memory devices." Appx2287.

Moreover, Google ignores and thus fails to show error in the Board's reliance on contrary statements from Netlist's expert. Appx142-143 (citing Appx929-933;

Appx6682; Appx16819-16827). Netlist's expert repeatedly explained that "it would not be obvious to a POSITA to modify Amidi's system by providing the bank address signals to the CPLD device," because "Amidi consistently and unambiguously teaches" using only other signals. Appx929-933; Appx16822-16823, Appx16825. This Court defers to the Board's decision as factfinder in resolving such a "battle of the experts." *MeadWestVaco v. Rexam Beauty & Closures*, 731 F.3d 1258, 1269 (Fed. Cir. 2013); *Elbit*, 881 F.3d at 1358. By leaving this testimony and the Board's crediting of it unchallenged in the opening brief, Google forfeited any challenge to it. *SmithKline*, 439 F.3d at 1319.

C. Even Were The Court To Find Prejudicial Error, Remand Would Be Required

Were the Court to alter the Board's claim construction or hold the Board lacked substantial evidence for a finding, a remand would be required. Google and Inphi ask for reversal, but ignore that the Board must determine obviousness under the proper construction and based on all underlying factual issues in the first instance. The Board's finding that no prior art discloses or suggests the claimed "logic element" under the adopted construction was sufficient to find all appealed claims patentable. The reverse is not true, because to find the claims unpatentable as obvious the Board must address all claim limitations, the "invention as a whole." 35 U.S.C. § 103. That includes the register limitation, which Netlist amended when

it amended the "logic element" limitation. Appx16804. The Board's decisions never address whether the prior art discloses a register as amended. Appx109-166.

In addition, to hold the claims unpatentable as obvious the Board also would need to address other subsidiary factual issues: "An obviousness determination requires finding that a person of ordinary skill in the art would have been motivated to combine or modify the teachings in the prior art and would have had a reasonable expectation of success in doing so." *OSI Pharm. v. Apotex*, 939 F.3d 1375, 1382 (Fed. Cir. 2019) (citation omitted). The Board never addressed whether skilled artisans would have had a reasonable expectation of success in modifying the prior art to arrive at the claimed invention. Appx109-166.

CONCLUSION

For the foregoing reasons the Court should affirm the Board's decisions holding Netlist's claims patentable.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that I electronically filed the foregoing with the Clerk of the Court for the United States Court of Appeals for the Federal Circuit by using the CM/ECF system on December 12, 2019.

I certify that all participants in the case are registered CM/ECF users and that service will be accomplished by the CM/ECF system.

Dated: December 12, 2019

/s/ Seth W. Lloyd
Seth W. Lloyd

CERTIFICATE OF COMPLIANCE WITH FEDERAL CIRCUIT RULE 28.1

This brief complies with the type-volume limitation of Rule 28.1(b)(2) of the Federal Circuit Rules because it contains 13,972 words, excluding the parts of the brief exempted by Fed. R. App. P. 32(f) and Federal Circuit Rule 32(b), as determined by the word-counting feature of Microsoft Word.

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Dated: December 12, 2019

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